IN THE CLAIMS

Please cancel claims 45-47 without prejudice and add new claims 48-72.

31. (Currently Amended) A method of forming a transistor comprising:

forming a narrow bandgap semiconductor film on an insulating substrate;

forming a gate dielectric layer on said narrow bandgap semiconductor film;

forming a gate electrode on said gate dielectric; and

forming a pair of said source/drain regions adjacent to said narrow bandgap semiconductor film; wherein said gate electrode and gate dielectric is formed over a portion of said source/drain regions.

32. (Original) The method of claim 31 wherein said narrow bandgap semiconductor film has a bandgap of less than or equal to 0.7 eV.

33. (Currently Amended) The method of claim 32 wherein said narrow bandgap semiconductor film is selected from the group consisting of InAs, PdTe and InSb.

34. (Original) The method of claim 32 wherein said source/drain regions are formed from a semiconductor film having a larger bandgap ~~then~~ than said narrow bandgap semiconductor film.

35. (Original) The method of claim 31 wherein said source/drain regions are formed from a compound semiconductor.

36. (Currently Amended) The method of ~~claims~~ claim 34 wherein said semiconductor film of said source/drain regions is selected from the group consisting of InAlSb, ~~InP,GaSb,~~ InP, GaSb, GaP, and GaAs.

37. (Original) The method of claim 31 wherein said source/drain regions are formed from a metal film.

38. (Original) The method of claim 37 wherein said metal film forms a Schottky barrier with said narrow bandgap semiconductor film.

39. (Currently Amended) The method of claim 37 wherein said metal film is selected from the group consisting of titanium nitride, tantalum nitride and ~~hefium~~ hafnium nitride.

40. (Original) The method of claim 31 wherein said gate dielectric layer comprises a high dielectric constant film.

41. (Original) The method of claim 31 wherein said gate electrode comprises a metal film.

42. (Original) A method of forming a transistor comprising:

forming an InSb alloy film on an insulating substrate;

forming a high dielectric constant gate dielectric film on said InSb alloy film;

forming a metal gate electrode on said gate dielectric layer; and

forming a pair of source/drain regions on opposite sides of said gate electrode on said insulating substrate.

43. (Original) The method of claim 42 wherein said source/drain regions are formed from a metal film.

44. (Currently Amended) The method of claim 42 wherein said source/drain regions are formed from a semiconductor film with a larger bandgap energy than said InSb alloy film.

45. (Cancelled)

46. (Cancelled)

47. (Cancelled)

48. (New) A method of forming a transistor comprising:

forming a narrow bandgap semiconductor film on an insulating substrate;

forming a gate dielectric layer on said narrow bandgap semiconductor film;

forming a gate electrode on said gate dielectric layer; and

forming a pair of source/drain regions adjacent to said narrow bandgap semiconductor film; wherein said source/drain regions are formed from a semiconductor film having a larger bandgap energy than said narrow bandgap semiconductor film.

49. (New) The method of claim 48 wherein said source/drain is formed from a semiconductor film with a bandgap energy at least 0.2 eV greater than the bandgap energy of said narrow bandgap semiconductor film.

50. (New) The method of claim 48 wherein said source/drain region is

formed from a semiconductor film with a bandgap energy at least 0.5 eV greater than the bandgap energy of said narrow bandgap semiconductor film.

51. (New) The method of claim 48 wherein said large bandgap semiconductor film of said source/drain regions is selected from the group consisting of InAlSb, InP, GaSb, GaP, and GaAs.

52. (New) A method of forming a transistor comprising:

forming a narrow bandgap semiconductor film on an insulating substrate;

forming a high k gate dielectric layer on said narrow bandgap semiconductor film;

forming a gate electrode on said high k gate dielectric; and

forming a pair of source/drain regions adjacent to said narrow bandgap semiconductor film.

53. (New) The method of claim 52 wherein dielectric constant of high k dielectric is greater than 9.0.

54. (New) The method of claim 52 wherein dielectric constant of high k dielectric is greater than 50.

55. (New) The method of claim 52 wherein said high k dielectric film is selected from the group consisting of lead zirconate titanate (PZT) and barium strontium titanate (BST).

56. (New) The method of claim 52 wherein said high k dielectric film comprises a metal oxide dielectric.

57. (New) The method of claim 56 wherein said metal oxide dielectric is selected from the group consisting of tantalum pentaoxide, titanium oxide, hafnium oxide, zirconium oxide, and aluminum oxide.

58. (New) The method of claim 52 wherein said high k dielectric film is formed by a low temperature process.

59. (New) The method of claim 58 wherein said high k dielectric film is formed at temperature between 200-500°C.

60. (New) The method of claim 58 wherein said high k dielectric film is formed by a method selected from the group consisting of vapor deposition and sputtering.

61. (New) The method of claim 52 wherein said source/drain regions are formed from semiconductor film with a bandgap energy greater than bandgap energy of narrow semiconductor film.

62. (New) The method of claim 52 wherein said source/drain regions are formed of a metal film.

63. (New) The method of claim 62 wherein said metal film is selected from the group consisting of platinum (Pf), aluminum (Al), and gold (Au).

64. (New) A method of forming a transistor comprising:
forming a narrow bandgap semiconductor film on an insulating substrate;

forming a mask on said narrow bandgap semiconductor film; wherein said mask defines a channel region of said transistor;

removing said narrow bandgap semiconductor film in alignment with said mask to remove said narrow bandgap semiconductor film from subsequent source/drain regions and thereby forming a channel region;

removing said mask from channel region;

forming a source/drain film on said insulating substrate and over narrow bandgap semiconductor film;

planarizing said source/drain film whereby a portion of said source/drain film is removed and remaining said source/drain film is substantially planar with the top surface of said narrow bandgap semiconductor film;

forming a gate dielectric film on said narrow bandgap semiconductor film;

forming a gate electrode film over said gate dielectric;

etching said gate electrode film and gate dielectric film to form a gate electrode and gate dielectric.

65. (New) The method of claim 64 wherein said narrow bandgap semiconductor film is formed on said insulating substrate by a wafer bonding technique.

66. (New) The method of claim 64 wherein said narrow bandgap semiconductor film comprises InSb.

67. (New) The method of claim 64 wherein said insulating substrate consists of a silicon substrate and buried oxide layer.

68. (New) The method of claim 67 wherein buried oxide layer comprises silicon dioxide.

69. (New) The method of claim 64 wherein said source/drain film is a compound semiconductor of the selected group consisting of InAlSb, InP, GaSb, GaP, and GaAs.

70. (New) The method of claim 64 wherein said source/drain are formed of a metal film.

71. (New) The method of claim 64 wherein said gate dielectric film is a high dielectric film such as a metal oxide dielectric.

72. (New) The method of claim 64 wherein said gate electrode film is a metal film from the selected group consisting of tungsten, titanium, and tantalum.

Drawing Amendment

The Examiner has objected Figure 1 for failing to designate it as "Prior Art" according to MPEP § 608.02g. The Applicants have made the change in compliance with patent examiner procedures. A replacement sheet, disclosing changes to the application drawings, is attached to this amendment document entitled "Replacement Sheet". Therefore, Applicants respectfully request the Examiner to withdraw this objection.